Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-44. (Canceled)

45. (Previously Presented) A pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream, comprising:

a correlator to correlate a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence to modulate the original bit stream;

a phase controller, coupled to the correlator to histogram the correlator output of the correlator over the plurality of bit periods, wherein the phase controller includes a plurality of counters to histogram the correlator output over all sample positions in a bit period for the plurality of consecutive bit periods, each of the counters corresponding to each of the sample positions within the bit period and, wherein each of the counters is incremented when a corresponding thresholded correlator output generates a spike at the corresponding sample position; and

a bit clock generator, coupled to the phase controller, to generate a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator to use the histogram of

the correlator output to select/adjust the sample position for the bit clock, wherein the bit clock generator adjusts the sample position of the bit clock to a position where the corresponding counter exceeds a threshold and, wherein the bit clock generator retains the same sample position of the bit clock where no counters exceed the threshold.

46. (Previously Presented) The circuit of claim 45, wherein the phase controller includes a plurality of counters to histogram the correlator output over a finite window of sample positions for the bit clock.

47. (Previously Presented) The circuit of claim 45, wherein the phase controller histograms the correlator output for a finite number of bit periods and restarts histogramming after the finite number of bit periods.

48. (Previously Presented) The circuit of claim 45, wherein the phase controller histograms continuously by digitally low pass filtering the correlator output.

49. (Previously Presented) A pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream comprising:

a correlator to correlate a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence to modulate the original bit stream;

a phase controller, coupled to the correlator to histogram the correlator output of the correlator over the plurality of bit periods;

a bit clock generator, coupled to the phase controller, to generate a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator to use the histogram of the correlator output to select/adjust the sample position for the bit clock; and

a comparator to compare the correlator output to a threshold and to generate a thresholded correlator output, wherein the phase controller histograms the thresholded correlator output with a plurality of counters.

50. (Previously Presented) The circuit of claim 49, wherein the phase controller comprises a plurality of accumulators to histogram the correlator output directly.

51. (Original) The circuit of claim 49, wherein the bit clock is based on the histogram of the counters that exceed a preset threshold.

52. (Original) The circuit of claim 50, wherein the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

53. (Previously Presented) The circuit of claim 49, wherein the bit clock is based on a calculated average sample position for the bit clock.

54. (Previously Presented) A communication system, comprising:

a transmitter to modulate an original bit stream into a transmitted chip stream by a pseudo-noise sequence, the transmitted chip stream to be transmitted to a receiver via a transmission media;

the receiver coupled to receive a chip stream; and

a clock recovery circuit coupled to the receiver, the clock recovery circuit to recover the original bit stream from the received chip stream, comprising:

a correlator to correlate a pseudo-noise sequence with the received chip stream and to generate a correlator output, the pseudo-noise sequence modulating the original bit stream;

a phase controller, coupled to the correlator, to histogram the correlator output over the plurality of bit periods; and

a bit clock generator, coupled to the phase controller, to generate a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator to use the histogram of the correlator output to select/adjust the sample position for the bit clock.

55. (Original) A computer program storage medium readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

56. (Original) A computer data signal embodied in a carrier wave readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

57. (New) The medium of claim 55, wherein maintaining the history of correlation comprises histogramming a correlator output over all possible sample positions for the bit clock.

58. (New) The medium of claim 55, wherein maintaining the history of correlation comprises histogramming a correlator output over a finite window of sample positions for the bit clock.

59. (New) The medium of claim 55, wherein maintaining the history of correlation comprises histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

60. (New) The medium of claim 55, wherein maintaining the history of correlation comprising histogramming the correlator output directly with a plurality of accumulators.

61. (New) The medium of claim 60, wherein synchronizing the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

62. (New) The medium of claim 55, wherein synchronizing the bit clock is based on a calculated average sample position for the bit clock.

63. (New) The medium of claim 55, further comprising providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

64. (New) The carrier wave of claim 56, wherein maintaining the history of correlation comprises histogramming a correlator output over all possible sample positions for the bit clock.

65. (New) The carrier wave of claim 56, wherein maintaining the history of correlation comprises histogramming a correlator output over a finite window of sample positions for the bit clock.

66. (New) The carrier wave of claim 56, wherein maintaining the history of correlation comprises histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

67. (New) The carrier wave of claim 56, wherein maintaining the history of correlation comprising histogramming the correlator output directly with a plurality of accumulators.

68. (New) The carrier wave of claim 56, wherein synchronizing the bit clock is based on a calculated average sample position for the bit clock.

69. (New) The carrier wave of claim 64, further comprising providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.